2. Please replace the paragraph beginning on page 5, line 23, with the following rewritten paragraph:

-- Caching and pre-fetching reduce the initial latency and subsequent latency. After a bus-to-memory read stream is completed, the pre-fetched data are kept in a read data queue. If the consecutive bus-to-memory read is a follow-on to the initial read, the read cycle continues from where the initial read left off. For subsequent data transfers, a watermark level is determined by calculating the amount of data that could have been transferred during the latency time on the bus interface. This is the amount of data that needs to be pre-fetched to keep a continuous data transfer stream. By delivering data continuously from the local data queue independently of the memory, latency due to subsequent data transfers is reduced.--

3. Please replace the sentence beginning on page 7, line 16, with the following rewritten sentence:

-- The bus access circuit 125 includes a peripheral bus controller 210, a pre-fetcher 215, a queue controller 230, a data coherence controller 250, a scheduler 260, a data mover 270, and a data queue 280.--

4. Please replace the paragraph beginning on page 7, line 23, with the following rewritten paragraph:

-- The peripheral bus controller (PBC) 210 receives control and request signals from the peripheral bus and interfaces to the pre-fetcher 215 and the queue controller (QC) 230. The PBC 210 decodes the access request and determines if the access request is valid. If the access request is valid, the PBC 210 forwards the access request to the RPG 220 and to the QC 230. The QC 230 determines if there is a hit or a miss. The hit/miss detector can be performed by comparing the address of the request with the address range of the data queue. The RPG 220 returns a control signal to the PBC 210 for moving data from the cache queue 280 to the peripheral bus. Upon receipt of the control signal from the RPG 220, the

PBC 210 sends a command to the QC 230 to start the data transfer from the data queue 280 to the peripheral bus.--

5. Please replace the sentence beginning on page 8, line 13, with the following rewritten sentence:

--The watermark monitor 225 determines if the amount of data in the data queue 280 is above a pre-determined level.--

6. Please replace the sentence beginning on page 8, line 17, with the following rewritten sentence:

If the request results in a hit, (e.g., the requested data item is in the data queue 280), the RPG 220 sends a control signal to the PBC 210 to enable the PBC 210 to start data transfer from the data queue 280.

7. Please replace the paragraph beginning on page 9, line 5, with the following rewritten paragraph:

The queue controller (QC) 230 receives control information from the PBC 210 and interacts with the watermark monitor 225, the data mover 270, and the cache queue 280. The QC 230 manages the data allocation for the data queue 280 by monitoring the amount of data in the data 280. This information is forwarded to the data mover 270 for controlling data movement from the memory to the data queue 280. The QC 230 also controls the data movement from the data queue 280 to the peripheral bus by responding to the status information provided by the PBC 210.--

8. Please replace the paragraph beginning on page 9, line 21, with the following rewritten paragraph:

The data coherence controller (DCC) 250 receives a control signal, (e.g., a clear data signal), from the RPG 220 and forward to the data mover 270, which in

turn forwards to the QC 230. The QC 230 performs a data purge operation upon receiving this clear data signal.--

9. Please replace the paragraph beginning on page 10, line 18, with the following rewritten paragraph:

--The data queue (DQ) 280 stores data items from the memory as transferred by the DM 270. The amount of data in the DQ 280 is monitored by the QC 230. The data items stored in the DQ 280 are read out to the peripheral bus when the QC 230 determines that there is a hit upon receiving a read request from the bus as generated by the PBC 210, or when the missed data are transferred from the memory to the DQ 280.--

10. Please replace the paragraph beginning on page 10, line 24, with the following rewritten paragraph:

--Activities in the bus access circuit 125 includes bus decode by the PBC 210, cache check by the QC 230, request generation by the RPG 220, data move and purging by the scheduler 260 and the DM 270, and data delivery and caching by the QC 230 and the DQ 280. These activities can be illustrated in a timing diagram for a particular access request.--

11. Please replace the sentence beginning on page 17, line 22, with the following rewritten sentence:

--Next, the process 650 stores the read data in the read data queue (Block 870) and is then terminated.--

IN THE DRAWINGS

Please accept the accompanying copy of the Request for Approval of Drawing Changes.